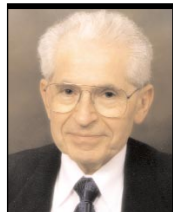


# M I C R O P R O C E S S O R

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THE INSIDER'S GUIDE TO MICROPROCESSOR HARDWARE



THE EDITORIAL VIEW

## SHARING YOUR EXPERIENCE

*MPR Welcomes Technical and Business Contributions*

*By Max Baron {4/28/08-02}*

Today's analysis of new processor architectures and configurations has taken us far from the now muted battle between RISC and CISC architectures, the topic that has placed *Microprocessor Report* on the global map and made it an indispensable publication for

designers and technical business managers.

The world has changed: *EDN's* 2007 microcontroller and microprocessor directory counts in its database almost 1,000 cores and chips from 70 vendors.

The DSP was almost unknown back in the days when CISC and RISC processors were battling one another. This year's *EDN* DSP database includes more than 200 products offered by 45 vendors.

We must add to these already large numbers our estimate of 500–600 implementations that have not been made public. These would be employing custom ISAs created recently by unknown inventors using configurable and extensible technologies offered by companies such as Altera, ARC, MIPS, Tensilica, and Xilinx.

At *MPR*, as we continue to review processor cores and countless architecture combinations, we see SoCs designed to match system-external specifications that are providing best features and performance for their intended applications. The days are gone when all we needed to review were the ISA and the ingenious implementation details that gave the processor its performance in executing applications and, more recently, its power efficiency.

We must now ask how the processor or SoC will perform in a complete system and estimate whether the chip's or core's enhancements can be really useful in the system it targets.

We remember Transmeta's innovations in processor power consumption that became less significant when employed in a system that had to power a monitor screen, hard drive, and local memory. Today, to make sense, we have no choice but to look beyond the processor and the workload it must execute—to see if the rest of the system can justify selecting an existing processor or a custom SoC's design. An example of a simple question to ask would be the following: Will system designers choose a processor that can handle 20GB/s of data for a system whose communications with the external world can provide it with less than 1.0Gb/s? (Lowercase "b" is intentional.)

The second decade of the 21st century is almost upon us. The variety of systems and processors that must fit each other efficiently will continue to increase every day, and the expertise of the design teams involved must be equal to the challenge. Processor designers and managers will profit from exposure to system hardware and software design considerations. And vice versa: system-design experts can take advantage of information highlighting accomplishments in silicon. At *MPR*, in addition to broadening the scope of our analysis, we believe it has become important to encourage processor designers, system designers, system programmers, and engineering managers to share their experiences and views via the pages of *MPR*.

During the past few months readers of *MPR* have noticed contributed articles from experienced professionals

such as Harlan McGhan, Grant Martin and Steve Leibson, and Frank Altschuler and Bruno Zoppis. The articles were part of our probe designed to provide a wide variety of information to our readers, adding to the content of *MPR*, which continues to publish technical reviews written by our technical and business staff analysts. The probe, we believe, showed us that our readers benefited from information selected from a wider palette of technical disciplines. Now, we would like to extend our invitation to hardware and software practicing professionals in academic and engineering positions.

In-Stat, publisher of *Microprocessor Report* and electronic business analysis, invites you to submit proposals for in-depth technical and technical-business articles to be published on the *MPR* website and in hardcopy issues of *Microprocessor Report*. The articles must represent the unbiased views and opinions of their writers. Articles accepted for publication will not be self-serving or favor any company or its product—they will, however, bring credit in print to the writer and company employing him/her.

A short nonexhaustive list of topics of interest includes the following:

- Advances in computer technology and architecture
- Advances in semiconductor technology
- Issues in designing and programming multiple-core and massively parallel architectures
- Data-intensive processing chips and IP aimed at video, imaging, audio, graphics, and image recognition
- Lowering power via semiconductor technology, physical design, architecture, and system and application software
- General-purpose processors for PCs, workstations, and servers
- General-purpose low-power embedded cores and chips
- General-purpose high-performance embedded cores and chips
- Imaging and video DSP

- Consumer electronics and other application-specific processors
- Advanced microcontroller designs
- Designs employing processors and DSP implemented in FPGA and CPLD technologies
- Processors and SoCs in automotive applications
- MP3 and video recorders and players in home and mobile applications
- Cellular phones
- Supercomputing chips and workstations
- Graphics
- Application-specific platforms: the cores, the chips, and the software that must make them work
- Multicore processors and enabling technologies
- IP and tools for system-on-chip (SoC) design

Accepted proposal authors will be provided with technical and writing style help and guidance by the staff of *MPR*. Aside from the worldwide visibility provided by the English language, very interesting *MPR* articles may be translated for publication in countries where Reed Business Information is publishing localized versions of *EDN* and other magazines.

Proposals for articles are welcome at any time.

Please send proposals and questions about technical content and topics to Max Baron. Phone in the U.S.: 408.773.9677. Email: [mbaron@reedbusiness.com](mailto:mbaron@reedbusiness.com) and [MaxMBaron@aol.com](mailto:MaxMBaron@aol.com).

Please copy proposals and direct all other questions to Ms. Sally Pena. Ms. Pena's phone in the U.S.: 408.345.1622. Email: [sally.pena@reedbusiness.com](mailto:sally.pena@reedbusiness.com).

The analyst team and editorial staff at *MPR* wishes our authors the best of success! ♦

